Enhanced Spatial PEB Uniformity through a Novel Bake Plate Design

Qiaolin Zhang[a,b]
qzhang@eecs.berkeley.edu
Paul Friedberg[b], Kameshwar Poolla[a,b], Costas Spanos[b]
a) UC Berkeley, Department of Mechanical Engineering
b) UC Berkeley, Department of Electrical Engineering and Computer Sciences

Abstract

CD-PEB temperature experiments show that post-exposure bake (PEB) temperature non-uniformity (both in steady-state and transient phases) impacts across-wafer CD uniformity [1]. Continued improvement in CD uniformity requires across-wafer temperature uniformity for the *entire* PEB cycle. This poses new challenges for the design of PEB thermal modules. This paper proposes a novel PEB thermal module design together with a novel robust control methodology to address this challenge. The proposed PEB thermal module relies on an intelligent wafer "carrier", which includes an array of Peltier devices and thermal sensors, so that the thermal uniformity of the wafer/carrier assembly can be continuously measured and controlled. The wafer resides in the carrier during the entire thermal processing cycle – transport, chill, and bake. This design enables the system comprising the wafer and the carrier to be in continual closed-loop control. As a result, thermal fluctuations due to PEB plate dynamics are largely eliminated and sharp temperature non-uniformities that result from introducing a wafer into the PEB process are greatly reduced. In essence, our design offers a thermally regulated mini-environment for silicon wafers during the entire PEB cycle. Simulation results show that this design can achieve temperature uniformities of less than 0.1°C across the wafer, through the entire PEB cycle (transient, as well as steady state). Given that today's state of the art bake plates achieve close to 0.1°C uniformity only in steady-state, and may have several degrees non-uniformity during the transient, this would result in a significant improvement in across-wafer CD uniformity. The same system can be used if there is a need to customize the PEB temperature history across the wafer in order to cancel out other sources of CD non-uniformity.

Keywords

PEB temperature non-uniformity, heating and cooling transient, CD variation, Peltier device, robust control, mini-environment

I. Introduction

As the semiconductor industry goes well beyond the 65nm technology node, control of gate critical dimension (CD) becomes increasingly important. In particular, regulating the across-wafer CD variation become crucial as it is a significant contributor to the overall CD variation error budget.

As lithography transitions to 193nm, the PEB step is becoming the major contributor of across-wafer CD variability. This is due both to the large PEB thermal sensitivity of 193nm resist and to the PEB temperature non-uniformity of modern wafer tracks. Both steady-state PEB temperature non-uniformity and transient PEB temperature non-uniformity significantly impact the CD uniformity [1,2,3]. Further reduction in across-wafer and wafer-to-wafer CD variation require exceptional across-wafer and wafer-to-wafer PEB temperature uniformity (< 0.1°C) for the entire PEB cycle, *including* the transient phases. Conventional state-of-the-art wafer tracks cannot deliver such performance, particularly during the heating and cooling transients. This is due to the inherent lack of thermal control during the transport phases at the beginning and the end of the PEB bake sequence.

In order to achieve less than 0.1°C temperature non-uniformity through the entire PEB cycle, we propose a novel PEB module design which integrates an intelligent wafer "carrier" as a thermal non-uniformity shield into conventional PEB module. The wafer being processed resides on the carrier during the entire PEB cycle. The carrier itself contains a controllable array of Peltier devices. We offer a robust control methodology to adaptively control the Peltier array to regulate the spatial temperature profile of the wafer at all times. As a result, the desired PEB temperature uniformity (or otherwise customized spatial/temporal thermal profiles) can be achieved during the entire PEB cycle, reducing both across-wafer and

wafer-to-wafer CD variability. Simulation results demonstrate the potential of the proposed approach.

II. PEB temperature non-uniformity and CD

While conventional PEB module designs emphasize steady-state temperature uniformity, transient PEB temperature also affects CD [2, 3]. This is because it is the total thermal dose absorbed by wafer that determines the chemical reaction rate of chemically amplified resist. The effect of transient PEB temperatures on CD uniformity is further corroborated by our experimental work [1]. We measure the across-wafer post-develop resist CD via CD-SEM and the across-wafer PEB temperature distribution for the entire PEB cycle via wireless sensor wafer from OnWafer Technologies [4]. Figures 1 and 2 show that both steady-state and transient PEB temperature profiles correlate significantly with the CD map.

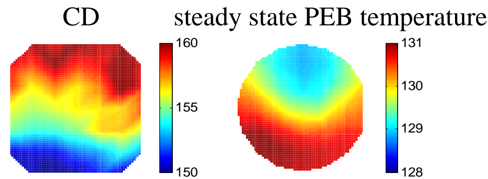


Fig. 1: AW CD and steady state PEB temperature signature (correlation =0.82).

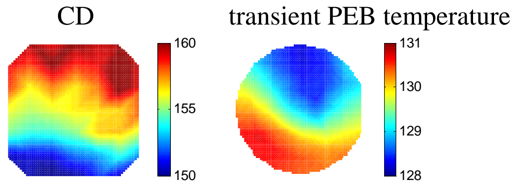


Fig. 2: AW CD and transient PEB temperature signature (correlation =0.73).

III. Conventional and Novel PEB module design

Even with state-of-the-art wafer tracks, the across-wafer PEB temperature range can be as much as 9°C during the heating and cooling transient and 0.7^{o}C during the steady-state [2], as shown in Figure 3. While better performance has been recorded, it is very difficult to achieve good uniformity, especially during the transient phase, due to the inherent lack of temperature control during wafer transport and heating and cooling transients.

More specifically, the bake step is conducted by transferring the cold wafer to the hot PEB bake plate and the chill step is conducted by transferring the hot wafer to a chill plate. These wafer transfers between plates abruptly change the dynamic system's thermal mass and behavior; as a result, the existing PID control methodology cannot deliver optimal control of PEB plate/wafer temperature. This leads to unacceptably large PEB temperature range especially during the transients.

In this work we propose a novel PEB bake/chill module, which relies on a special wafer carrier to transfer between heating and cooling plates. As shown in Figure 4, the smart wafer carrier consists of a top thin plate, a Peltier device array and a bottom thin plate. The wafer sits on the wafer carrier via proximity pins during the entire PEB heating/cooling cycle. Temperature sensors are embedded onto the top thin plate to measure the spatial PEB temperature. The Peltier devices function as heat pumps, to either heat or cool the wafer. This carrier gets transported from the wafer handling robot arm to the hot plate, and then to the chill plate. In this application the hot and chill plates do not need to achieve high levels of thermal uniformity or stability. In fact, simulations show that 5°C across-plate temperature range is acceptable. During the entire PEB cycle, the wafer is adaptively heated or cooled by the Peltier devices in a proximity mode. This ensures spatial uniformity, both in steady-state, and also during the rapid transients as the wafer/carrier assembly moves from one robot, to the hot plate and then to the chill plate.

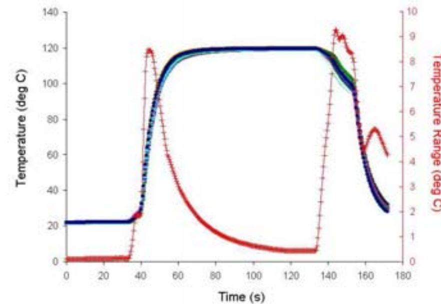


Fig.3: Across-wafer PEB temperature& temperature range during entire PEB cycle

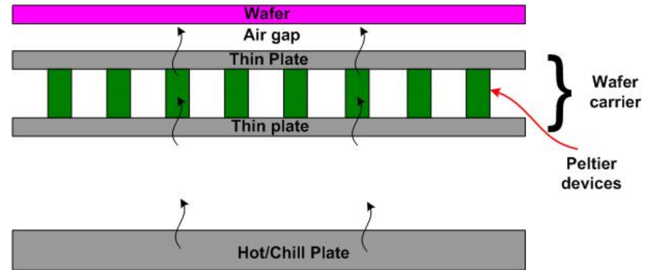


Fig. 4: Hardware setup of novel PEB thermal module

We propose a 6 radial zone design for the PEB bake plate (as shown in figure 5), configured by properly wiring the Peltier devices array. Different zone patterns that allow for radial asymmetries are also possible. The Peltier devices in each zone are connected in series, and the current for each one of the zone groups is individually controlled by a feedback controller using a robust control algorithm.

Figure 6 shows an example of the desired PEB trajectory for each zone of the top thin plate and wafer. The robotics transfers the exposed wafer onto the wafer carrier after the exposure, and the Peltier devices are adaptively actuated to maintain good across-plate/wafer initial temperature uniformity. The wafer carrier carrying the exposed wafer is transferred above the hot plate, and the Peltier devices

adaptively heat the top thin plate and wafer by conducting heat to the top thin plate and wafer, which ensures that temperature trajectory on each zone of the plate/wafer track the desired temperature trajectory during the heating transient and steady-state. After the wafer is baked at the desired temperature and time, the carrier and the wafer is moved away from the hotplate onto the chill plate, when the Peltier devices adaptively cool the top thin plate and wafer by pumping heat to the chill plate. During the entire PEB cycle (heating transient, steady-state and cooling transient), the DC current of Peltier devices of each zone is controlled based on the temperature feedback of temperature sensors mounted on the top thin plate. As a result, the PEB temperature trajectory of each zone will track the pre-designed desired PEB trajectory within ±0.05°C error bound.

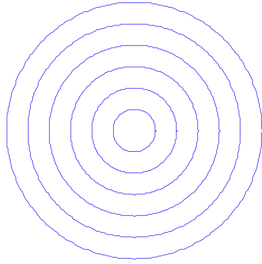


Fig. 5: 6-zone PEB bake plate

IV. Robust control methodology

PID control is widely employed in PEB bake plate modules in state-of-the-art wafer tracks. This control scheme is straightforward to implement but sensitive to modeling errors, drifts, and external disturbances. Indeed, the performance of these PID controllers does vary significantly across a wafer and from wafer to wafer. Thus the PID control strategy itself contributes to PEB temperature non-uniformity. We propose an alternate control methodology – *sliding mode control* [5]. This does not require a high fidelity system model and can be more robust to modeling errors and external disturbances.

The dynamic model for each zone of the top thin plate is:

$$m \cdot c_p \frac{dT}{dt} = -h(T - T_A) + b \cdot I^2 \cdot \mathrm{sgn}(I) - k_{air} \cdot (T - T_w) + d$$

T	top thin plate local temperature	
T_A	ambient temperature	
c_p	heat capacity of top thin plate	900 J/(kg.K)
m	mass (per zone) of top thin plate	0.14kg
h	heat transfer coefficient for heat loss to the ambient	0.02kW/K
b	heat transfer coefficient of Peltier device array	5.6kW/A^2
I	current through the Peltier array	
k_{air}	the thermal conductivity of air	0.08KW/K
d	approximate thermal disturbance	0.01kW

Table 1: Model parameters for each zone of top thin plate

The thermal model of the corresponding zone of wafer is:

$$m_w \cdot c_{pw} \frac{dT_w}{dt} = -h_w(T_w - T_A) + k_{air}(T - T_w) + d_w$$

T_w	wafer local temperature	
c_{pw}	heat capacity of silicon	700 J/(kg.K)
m_w	mass (per zone) of wafer	0.01kg
h_w	heat transfer coefficient for heat loss to the ambient	0.02kW/K
d_w	approximate thermal disturbance	0.01kW

Table 2: Model parameters for each zone of wafer

In reality, these dynamic models will have errors. This can be treated by allowing for all the parameters in these models to deviate from their nominal values. In our simulations, we will allow for ± 50% uncertainty in the parameter values. Sliding mode control is robust to bounded model error and bounded external disturbance [5] in the sense that the system output (PEB temperature) can track the pre-designed system output trajectory within a specified tracking error bound in spite of system model error and external disturbance. Figure 6 shows the pre-designed desired PEB trajectory for one PEB cycle. This is the target temperature trajectory for each zone of the top thin plate and the wafer.

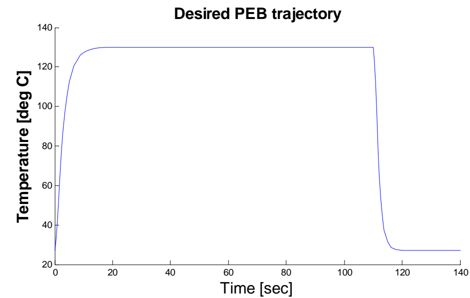


Fig. 6: Pre-designed desired PEB trajectory

By adaptively actuating the DC current in the Peltier device array, our proposed sliding mode control strategy enables temperature tracking for each zone to be within specified error bound. Also, the closed-loop performance is robust to model errors and disturbances such as wafer warpage.

V. Results

Simulation results using sliding mode control methodology on the proposed PEB thermal module indicate promise of our novel approach. Figure 7 shows that the tracking errors for all 6 zones remain within ±0.05°C throughout the entire PEB cycle. This implies that exceptional across-wafer and wafer-to-wafer temperature uniformity (0.1°C or better) is achieved throughout the PEB cycle. In addition, if CD uniformity rather than thermal uniformity is the desired

outcome, the trajectory of each of the zones can be tailored accordingly.

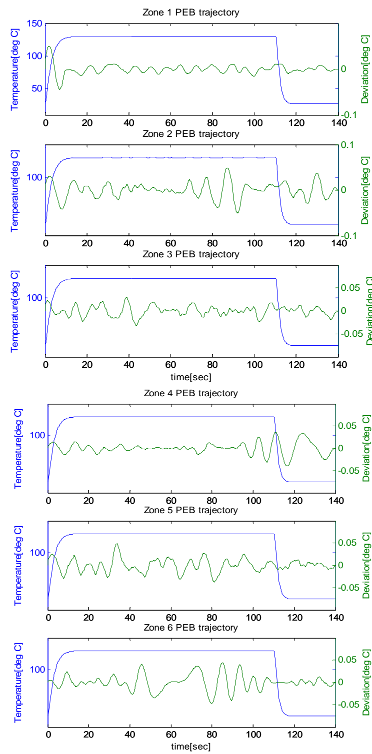
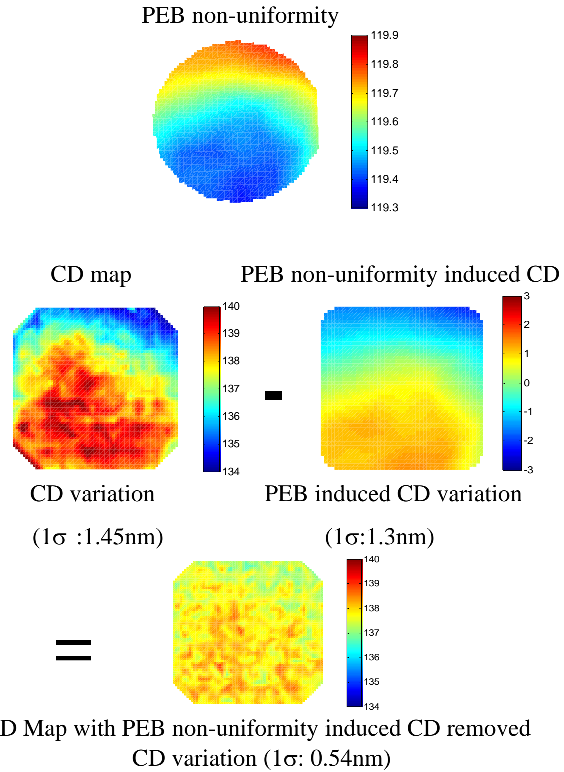


Fig. 7: Deviations of 6 zones' PEB temperature trajectories from the desired trajectory

Experimental investigation of 193nm process reveals that the PEB temperature non-uniformity is a major contributor to overall CD non-uniformity. PEB non-uniformity induced across-wafer CD variation can be estimated from the steady-state PEB temperature map and knowledge of the resist PEB thermal sensitivity (~7-10nm/^{o}C for 193nm resist). Subtracting this from the overall CD, lets us estimate the non-PEB-related CD variation.

Figure 8 exhibits the spatial detail of resolving the total CD variation into PEB related and non-PEB related components. Form this figure it is clear that PEB non-uniformity contributes the largest portion of the total CD variation. This confirms the significant opportunity in this paper – novel PEB thermal module design and robust control schemes can be key technologies in reducing CD variability.

Our simulation results demonstrate that ±0.05^{o}C temperature tracking errors across PEB trajectories are possible. This translates to ±0.4nm PEB-induced CD deviation ranges for 193nm resist. The implication of these simulations is that our novel PEB module and control scheme can offer 0.13nm PEB induced CD variations (1 σ) for 193nm process. This compares very favorable with 1.3nm (1 σ) PEB induced CD variation for state-of-the-art conventional wafer tracks. Finally, we remark that our proposed thermal module and control approach could also be used in other thermal processing step in IC manufacturing such as hard bake and soft bake to enhance thermal uniformity.



CD Map with PEB non-uniformity induced CD removed
CD variation (1σ: 0.54nm)

Fig. 8: Decoupling CD variation into PEB related components and non-PEB related components

ACKNOWLEDGEMENT

The authors would like to thank OnWafer Technologies for providing BakeTemp sensor wafers to support this project. This work was funded by Advanced Micro Devices, Applied Materials, Atmel, Cadence, Canon, Cymer, DuPont, Ebara, Intel, KLA-TENCOR, Mentor Graphics, Nikon Research, Novellus Systems, Panoramic Technologies, Synopsis, Tokyo Electron, and the UC Discovery Grant under contract number ELE03-10160, and by NSF under Grant ECS 03-02554.

REFERENCES

[1] Q. Zhang, P. Friedberg, et al., "Across Wafer CD Uniformity Enhancement through Control of Multi-zone PEB Profiles", Metrology, Inspection, and Process Control for Microlithography XVIII, SPIE 5375, Feb. 2004.
[2] P. Friedberg, C. Tang, et al., "Time-based PEB adjustment for optimizing CD distributions," Metrology, Inspection, and Process Control for Microlithography XVIII, SPIE 5375, Feb. 2004.
[3] D. Steele, A. Coniglio and etc, "Characterizing Post Exposure Bake Processing for Transient and Steady State Conditions, in the Context of Critical Dimension Control" Metrology, Inspection, and Process Control for Microlithography XVI, SPIE 5375, Feb. 2002.
[4] www.onwafer.com

[5] Jean-Jacques E. Slotine and Weiping Li, “Applied Nonlinear Control”, Prentice Hall, 1991.